C1 amd

33. (Amended) The memory, as set forth in claim 31, wherein the first line is disposed in a window formed in a dielectric layer disposed over the substrate.

35. (Amended) The memory, as set forth in claim 31, wherein the layer of a second conductive material is deposited on the first line using an immersion plating technique.

C2

36. (Amended) The memory, as set forth in claim 31, wherein the second conductive material comprises at least one of silver and gold.

37. (Amended) The memory, as set forth in claim 31, wherein the chalcogenide material comprises germanium selenide having ions of the second conductive material therein.

39. (Amended) The electronic device, as set forth in claim 38, wherein the first line is embedded in the substrate.

C3

40. (Amended) The electronic device, as set forth in claim 38, wherein the first line is disposed in a window formed in a dielectric layer disposed over the substrate.

42. (Amended) The electronic device, as set forth in claim 38, wherein the layer of a second conductive material is deposited on the first line using an immersion plating technique.

C4

43. (Amended) The electronic device, as set forth in claim 38, wherein the second conductive material comprises at least one of silver and gold.

44. (Amended) The electronic device, as set forth in claim 38, wherein the chalcogenide material comprises germanium selenide having ions of the second conductive material therein.

Please add new claims 82-89 as follows:

82. (New) A memory cell comprising:

a first memory access line formed over a substrate, the first memory access line being formed of a first conductive material;

C5

a layer of a second conductive material disposed on the first memory access line, the second conductive material being different from the first conductive material;

a layer of a variable resistance material disposed on the layer of the second conductive material, wherein the variable resistance material is capable of changing in resistance in response to a voltage level applied thereto; and

a second memory access line formed over the layer of variable resistance material.

83. (New) The memory cell, as set forth in claim 82, wherein the first memory access line is disposed in a window formed in a dielectric layer disposed over the substrate.

84. (New) A memory cell comprising:

a first layer of dielectric material disposed over a substrate, the first layer of dielectric material having a first window formed therein;

C5 cont.

a first memory access line disposed in the first window, the first memory access line being formed of a first conductive material;

a second layer of dielectric material disposed over the first layer of dielectric material and on the first memory access line, the second layer of dielectric material having a second window therein, the second window exposing at least a portion of the first memory access line;

a layer of a second conductive material disposed in the second window on the first memory access line, the second conductive material being different from the first conductive material;

a layer of a variable resistance material disposed in the second window on the layer of the second conductive material, wherein the variable resistance material is capable of changing in resistance in response to a voltage level applied thereto; and

a second memory access line formed over the layer of variable resistance material.

85. (New) A memory cell comprising:

a first layer of dielectric material disposed over a substrate, the first layer of dielectric material having a first window therein;

a first memory access line disposed in the first window, the first memory access line being formed of a first conductive material;

a second layer of dielectric material disposed over the first layer of dielectric material and on the first memory access line;

C5 cont

a first layer of conductive material disposed over the second layer of dielectric material, the first layer of conductive material and the second layer of dielectric material having a second window therein, the second window exposing at least a portion of the first memory access line;

a layer of a second conductive material disposed in the second window on the first line, the second conductive material being different from the first conductive material;

a layer of a variable resistance material disposed in the second window on the layer of the second conductive material, wherein the variable resistance material is capable of changing in resistance in response to a voltage level applied thereto; and

a second memory access line formed over the layer of variable resistance material and over the first layer of conductive material.

86. (New) A memory comprising:

a memory array having a plurality of memory cells, each of the memory cells comprising:

a first memory access line formed over a substrate, the first memory access line being formed of a first conductive material;

a layer of a second conductive material disposed on the first memory access line, the second conductive material being different from the first conductive material;

a layer of a variable resistance material disposed on the layer of the second conductive material, wherein the variable resistance material is capable of changing in resistance in response to a voltage level applied thereto; and

a second memory access line formed over the layer of variable resistance.

87. (New) The memory as set forth in claim 86, wherein the first memory access line is embedded in the substrate.

88. (New) The memory as set forth in claim 86, wherein the first memory access line is disposed in a window formed in a dielectric layer disposed over the substrate.

89. (New) An electronic device comprising:

a processor;

a memory operatively coupled to the processor, the memory comprising a memory array having a plurality of memory cells, each of the memory cells comprising:

a first memory access line formed over a substrate, the first memory access line being formed of a first conductive material;

a layer of a second conductive material disposed on the first memory access line, the second conductive material being different from the first conductive material;

a layer of a variable resistance material disposed on the layer of the second conductive material, wherein the variable resistance material is capable of changing in resistance in response to a voltage level applied thereto; and

a second memory access line formed over the layer of variable resistance.